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CADENCE AND TERANETICS COLLABORATE ON DESIGN OF 10 GIGABIT ETHERNET CHIPS USING X ARCHITECTURE

*Networking Startup Adopts Cadence X Architecture Design Solution
To Fulfill Demanding Power Consumption Requirements*

SAN JOSE, Calif. and SANTA CLARA, Calif.—April 18, 2006—Cadence Design Systems, Inc. (NASDAQ:CDNS) and Teranetics, Inc. today announced a design collaboration for implementation of Teranetics' 10 Gigabit Ethernet (10GBASE-T) chips using the X Architecture. Teranetics has also joined the X Initiative as the latest member of the semiconductor design-chain consortium chartered with accelerating the availability and fabrication of the X Architecture.

Teranetics and Cadence's design collaboration leverages the significant reduction in power consumption enabled by the Cadence X Architecture design solution. Reducing power consumption is a key requirement for leading-edge 10GBASE-T chips to be deployed in data centers and enterprise networks.

"Teranetics specializes in high-performance silicon solutions for Ethernet networks and is committed to delivering 10 Gigabit/s over structured copper cabling to the enterprise market," said Sanjay Kasturia, chief executive officer of Teranetics. "We are very excited with the remarkable reduction in power consumption demonstrated by the Cadence X Architecture design solution and plan to leverage it for our designs at advanced process nodes."

"The Cadence X Architecture design solution provides an innovative and powerful way to optimize designs for today's challenging power, die-size and performance needs," said Kalyan Thumaty, vice president and general manager of X Architecture at Cadence. "Exciting startups like Teranetics working on leading-edge designs are employing X

Architecture for their chips. The compelling benefits, coupled with ease of adoption, make the Cadence X Architecture design solution an obvious choice for startups as well as leading semiconductor companies worldwide.”

The Cadence X Architecture design solution is the industry’s first physical design solution that enables the pervasive use of diagonal routes and employs the familiar netlist-to-GDSII flow. While leveraging Cadence’s industry-proven Manhattan implementation expertise, the solution draws on innovations in placement, routing, infrastructure and extraction technologies.

About the X Architecture

The X Architecture represents a new way of orienting a chip’s microscopic interconnect wires with the pervasive use of diagonal routes, in addition to traditional right-angle “Manhattan” routing. The X Architecture can provide significant improvements in chip area, performance, power consumption and cost, by enabling designs with significantly less wirelength and fewer vias (the connectors between wiring layers).

About Teranetics

Teranetics, Inc. is a leading developer of semiconductors solutions for physical layer connectivity. The company specializes in ultra high performance mixed analog digital circuits and signal processing techniques. The company’s products are designed to provide practical solutions for next generation networks. Teranetics is headquartered in Santa Clara, California. Additional company information is available at www.teranetics.com

About Cadence

Cadence enables global electronic-design innovation and plays an essential role in the creation of today's integrated circuits and electronics systems. Customers use Cadence software and hardware, methodologies, and services to design and verify advanced semiconductors, printed-circuit boards and systems used in consumer electronics, networking and telecommunications equipment, and computer systems. Cadence reported 2005 revenues of approximately \$1.3 billion, and has approximately 5,000 employees. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More

information about the company, its products, and services is available at www.cadence.com.

About the X Initiative

The X Initiative, a group of leading companies from throughout the semiconductor industry, is chartered with accelerating the availability and fabrication of the X Architecture, a revolutionary interconnect architecture based on the pervasive use of diagonal routing. The X Initiative's five-year mission is to provide an independent source of education about the X Architecture, to facilitate support and fabrication of the X Architecture through the semiconductor industry design chain, and to survey usage of the X Architecture to track its adoption. Representing leaders spanning the entire design-to-silicon supply chain, X Initiative members include: Applied Materials, Inc.; ARM; ASML Netherlands B.V.; ATI Technologies Inc., Cadence Design Systems, Inc.; Canon U.S.A. Inc.; Dai Nippon Printing (DNP); GDA Technologies, Inc.; HPL Technologies, Inc.; Hoya Corporation; IN2FAB Technology Ltd.; Infineon Technologies AG; JEOL, Ltd.; KLA-Tencor Corporation; Leica Microsystems AG; Matsushita Electric Industrial Co., Ltd.; MicroArk Co. Ltd.; Nikon Corporation; NuFlare Technology Inc.; PDF Solutions, Inc.; Photronics, Inc.; Prolific Inc.; RUBICAD Corporation; Sagantec; Sanyo Electric Co., Ltd.; Silicon Logic Engineering, Inc.; SiliconMap, LLC.; Silicon Valley Research Inc.; STMicroelectronics; Sycon Design, Inc.; Tanner EDA; Tensilica, Inc.; Teranetics Inc.; Toppan Photomasks, Inc.; Toppan Printing Co.; Toshiba Corporation; TSMC; UMC; Virage Logic, Inc.; Virtual Silicon Technology, Inc.; Zenasis Technologies, Inc.; and Zygo Corporation. Membership is open to all companies throughout the semiconductor design chain. Materials can be found at <http://www.xinitiative.com>.

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